In-Operando X-ray Diffraction Imaging of Thermal Strains in Fully Packaged Silicon Devices

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Abstract

The application of X-ray Diffraction Imaging to measure *in operando* thermal strains at individually powered components within fully packaged LM3046 silicon devices is described. It is shown that as the local strains increase with power dissipated, above a threshold power loading, the associated region of enhanced X-ray intensity increases monotonically. The changes in contrast in the image are discussed. Asterism in section topographs changes sign as the slit is moved across the component, consistent with lattice strain around the device due to the thermal expansion. Above a threshold power, this asterism increases linearly with power loading. By simultaneous measurement of the package surface temperature it is possible to deduce the local component temperature from the extent of the contrast in the X-ray image.

1. Introduction

As manufacturers seek to meet forthcoming challenges associated, for example, with healthcare and the Internet of Things, an increasing number of heterogeneously packaged chips are appearing on the market. This reflects the ongoing transition from “More Moore” (MM) to “More than Moore” (MtN) approaches [1,2] for next generation devices and systems. The development of heterogeneously integrated chip packages will play a leading role in this evolution, which will most likely see the convergence of packaging and system integration [3]. Examples include 2D, 2.5D and 3D on-package integration approaches, fan-out wafer level packaging, and embedded die [4]. In many instances these advanced packages consist of vertically stacked and interconnected multiple layers of silicon. As a result, there has been a drive both to reduce the thickness of the silicon die/wafers used as well as the total thickness of the package. The thin die are subject to warpage when packaged and this has been found to be particularly problematic in multiple chips stacks with through-silicon via interconnection [5]. However, the reduction in package thickness has enabled non-destructive transmission X-ray Diffraction Imaging (XRDI) techniques [6,7] to be employed to map quantitatively the wafer distortions [8,9] and under stressed operating conditions [10].

Silicon drive transistors can dissipate substantial energy and 0.5W is not atypical. It is known that the life of a device reduces by a factor of about 2 for every 10°C increase in operating temperature and that operation at over 175°C is likely to result in short-term failure. Monitoring of the outside of the package can give clues as to the internal temperature but there are some questions that are difficult to determine from such macroscopic measurements. These include the question of how localized are the strains associated with electrical overload of specific silicon bipolar junction transistors and what is the magnitude of

those strains? Does the thermal strain extend enough to warp the wafer macroscopically within its package? How to monitor the device temperature is a technical challenge.

The ability of X-rays of typically 30-40keV energy to penetrate fully encapsulated devices also opens up the possibility of using XRDI techniques to measure, *in operando*, the local strain associated with individual components on the die/wafer running under conditions of electrical overload. Modelling of device behaviour is sophisticated and detailed, but it does rely on experimental data relating to the actual operation of the device. As local thermal load generates local thermal strains, there are two options for sensors built into chip architecture. Inclusion of a diode close to the component under consideration allows a direct measurement of temperature to be recorded or fabrication of piezoelectric sensors on the wafer allows a direct measurement of strain to be obtained at that point. Neither technique is realistic if data from more than a few devices are required and both strategies add cost to manufacturing processes that are dependent on low margins and high volume to be commercially viable. As we show in this paper, XRDI, which is also known as X-ray Topography, enables local strains to be detected and identified at individual devices *in operando* in fully packaged chips. The technique is non-invasive and non-destructive.

2. Experimental Techniques

XRDI experiments have been performed on discrete n-p-n bipolar junction transistors fully encapsulated in a LM3046 chip package at the B16 beamline of the Diamond Light Source in Oxfordshire in the United Kingdom. Beamline B16 is a multi-purpose test beamline capable of being operated in white beam, "pink" beam or monochromatic mode. Technical details can be found on the Diamond Light Source website. We selected the LM3046 Small Outline Integrated Circuit (SOIC) transistor array because it is an inexpensive, ubiquitous, well-characterized 14 pin device that is widely commercially available. At a thickness of 1.5mm, this SOIC package is typically 70% less in thickness compared with dual in-line packages and is hence well suited to the present aim of establishing the viability of XRDI as a non-destructive, *in situ* monitor of the behaviour of powered devices inside fully encapsulated chip packages. The LM3046 device, and any equivalent variant, contains 3 bipolar transistors and a pair of transistors in a current mirror configuration. These are fabricated on a silicon die of area 1mm×1mm and 400μm thickness. The relative area of the package taken up by the die is revealed in the absorption radiograph of Fig. 1, taken with the full white beam of synchrotron radiation. There is of course no strain information in the radiograph but it gives a good indication of the relative absorption associated with the polymer packaging. This shows as a saturated white area in the image, contrasting with the encapsulated lead frame, which appears grey.

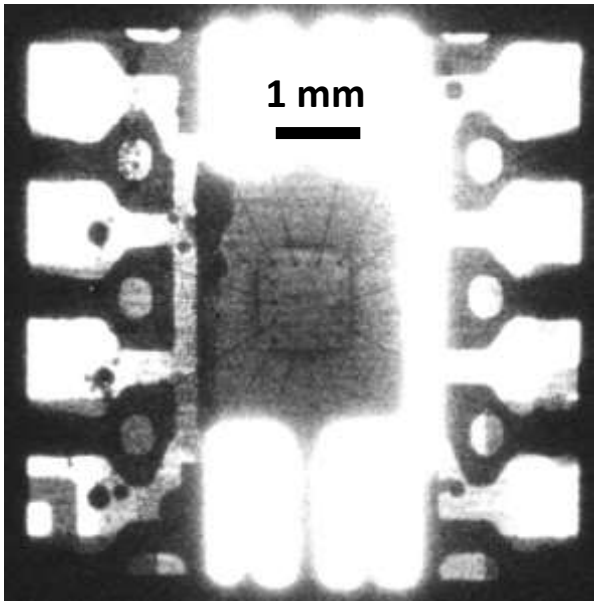


Fig. 1. Absorption radiograph showing the silicon wafer within the package and connecting wires to some of the 14 (dark in the image) pins on the LM3046. Note that the chip frame attenuates the X-ray beam quite strongly.

We report results for the three individual bi-polar n-p-n junction transistors under increasing load. The drive circuit was straightforward (Fig. 2), with the collector current I_C and collector-emitter voltage drop V_{CE} being measured independently and varied by a 0-1kΩ variable resistor. There was found to be a linear increase in the power dissipated in the transistor with decrease in load resistance. The specimen holder, which allowed the X-ray beam to pass unrestricted through the package, was similar to that described in reference [10].

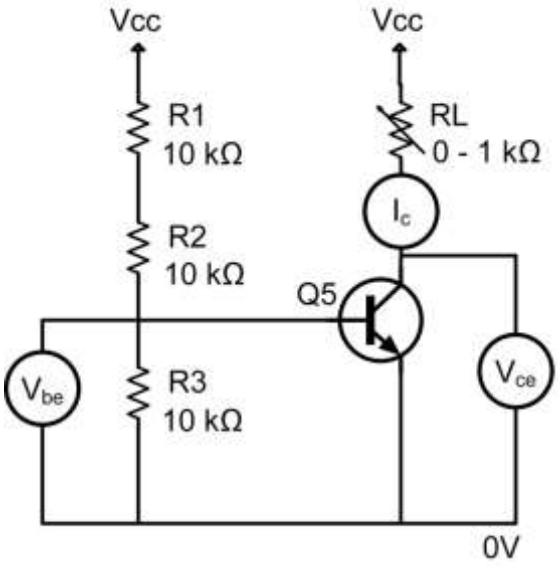


Fig.2. Drive circuit for an individual transistor (for example Q5) on the LM3046 device

We have driven the individual bipolar transistors under conditions of current beyond the normal working specification in order to image the associated thermal strains at specific devices. The temperature of the surface of the overall package was monitored using a Front Looking Infrared (FLIR) camera. Specifically, we used a Model FLIR i7 camera from FLIR

Systems AB which has a sensitivity of 0.1°C at 25°C. It was calibrated by attaching a type-K thermocouple in close proximity to the surface of the chip package and comparing the temperature data with that acquired using the FLIR camera. This confirmed the accuracy of the FLIR measurement of the package temperature to within 1°C. The efficacy of this method was also confirmed in reference [5]. All IR measurements were made at a single point, ambient being room temperature.

The single crystal wafer has been cut such that the surface is $(1\bar{1}1)$ oriented and one of the edges is parallel to the [110] direction, perpendicular to the surface normal. XRDI was performed in white beam mode, the wafer being tilted about the horizontal direction to set diffraction conditions for the 220 reflection in transmission mode. With a tilt of 6°, X-rays of primary energy of 31keV are diffracted and form the image which is recorded on an X-ray sensitive digital camera. The X-rays can be detected directly by the camera, as with the Photonic Science sCMOS camera which has a 7mm diameter field of view, 1920 × 1080 pixels, 14 bit dynamic range and approximately 3.2μm dimension optical pixels. Alternatively, for higher resolution but lower detection efficiency, the X-ray photons can be converted to visible light in a thin scintillator, this image then being magnified before being recorded. Such a method is used for the B16 beamline pco4000 CCD camera, manufactured by PCO AG of Kelheim, Germany, which has 4008 × 2672 pixels, 14bit dynamic range and where we chose the scintillator and optical magnification to give a 1μm pixel size on the camera. Further details can be found in references [8, 9] and [10]. All experiments were undertaken in standard multi-bunch mode with machine current of 300mA.

Because the image is formed from one Bragg diffracted beam, the image is sensitive to local strains in the wafer, unlike the radiograph of Fig.1. Despite there being strong attenuation in the package as a whole, the wafer is relatively thin (0.4mm) and the absorption in the silicon is low. At X-ray energy of 31keV the product of the silicon absorption coefficient μ and thickness t is found [11] to be $\mu t = 0.13$ and hence regions of local strain appear as regions of enhanced intensity in a white radiation X-ray Diffraction Image (topograph) due to the kinematical scattering in the distorted region compared with the dynamical diffraction in the undistorted material [6,7]. As the 220 reflection Bragg angle θ_B at 31keV energy is only 6°, $\tan\theta_B$ is small, namely 0.105. The effective misorientation $\Delta\theta$ of the deformed Bragg planes of spacing d, given by

$$\Delta\theta = \frac{\delta d}{d}\tan\theta_B \pm \delta\phi \qquad \text{Equation 1}$$

is thus dominated by the tilt of the planes $\delta\phi$, rather than the dilation δd. The distortion of the images therefore relates directly to the magnitude and sense of the Bragg plane tilt.

3. Results

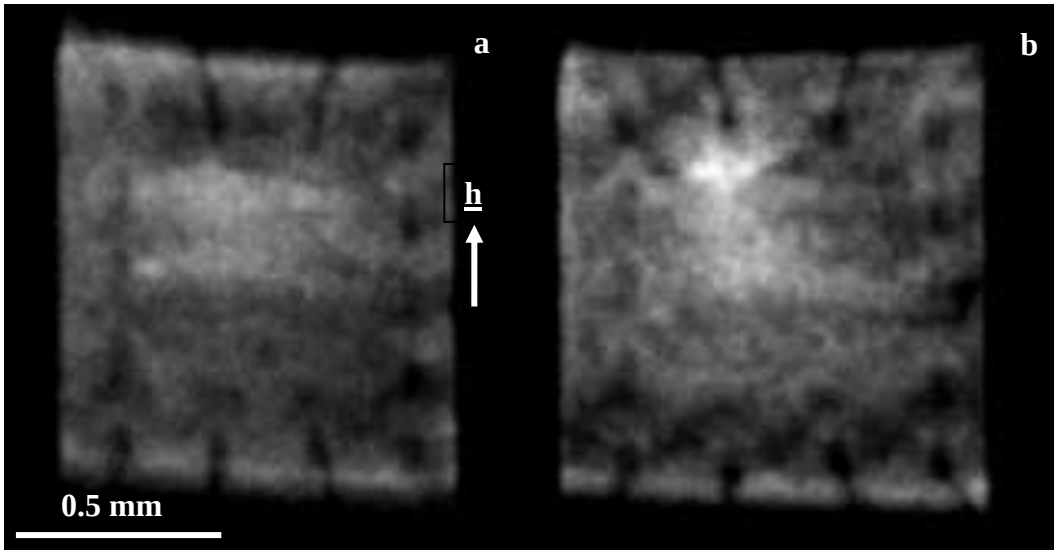
3.1 Full chip diffraction imaging

The first, and critically important result was that with the beam slits at 7 mm × 4.4 mm and thus the white X-ray beam illuminating the whole $1mm^2$ sample, there were no changes in the electrical characteristic compared with no X-ray illumination. Previous *in operando* XRDI of III-V based lasers [12,13] and ultra-fast recording of crack propagation in silicon [14] at the

European Synchrotron Facility had been undertaken using monochromatic radiation where the heat load was much smaller than in the white beam conditions which we used at the Diamond Light Source. Despite use of aluminium absorbers, the heat load on the sample under white beam illumination is substantial. However, no detectable electrical characteristic changes were observed when the beam shutter was opened and closed.

As illustrated in Fig. 3, no localised contrast associated with thermal strain at a specific device was observed for low power levels, but at higher levels, strong X-ray diffraction contrast in the form of enhanced intensity at the transistor was observed. With power dissipation of up to about 1.5W the image remained very similar to that recorded under zero load (Fig.3(a)). At 2.0W, enhanced intensity appears at the location of the relevant transistor (Fig 3.(b)). This is elongated in a direction perpendicular to the diffraction vector **h**, an effect that appears to be associated with the device geometry. Increase of power dissipation to 2.4W (Fig. 3(c)) results in extension of the contrast feature in the direction normal to the diffraction vector, there being no significant change in the diffraction vector direction (vertical in the figure.) Similar characteristics were found for transistors Q3 and Q4 in the package. The value of the load resistor, (or equivalently, power dissipation) in the transistor, at which the local image appeared was the same for each transistor and for equivalent transistors in different device packages. The length of the image was similar for equal load resistor values. Two examples of the whole sequence of increased power loading are given in video format in the Supplementary Information.

It is important to note that the diffuse nature of the image is intrinsic to the method and the strain distribution, not a limitation on the XRDI method. Use of the higher resolution pco4000 camera and scintillator gave similar diffuse images, there being no sharp definitive features. This differed significantly from the sharp, well resolved dislocation images, a few micrometres across, that were obtained from a SiC wafer using the same detector arrangement. However, as the intensity in the images was at the limit of the less efficient pco4000 camera and scintillator, data were taken on the Photonic Science sCMOS detector.



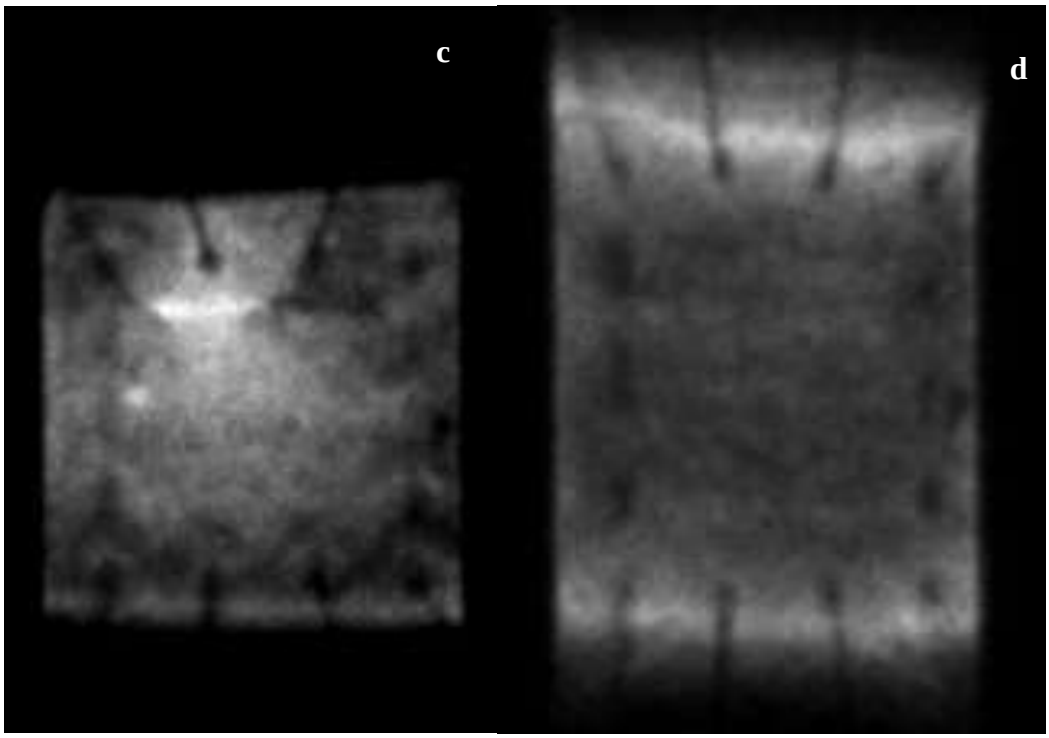


Fig. 3. 220 X-ray diffraction images of transistor Q5 in the LM3406 package under load (a) low load, i.e. 0-1.5W, (b) 2.0W, (c) 2.4W, (d) zero power after failure. Projection of the 220 diffraction vector **h** is vertical. Data taken with the Photonic Science sCMOS camera.

The power through the transistors was increased step-wise, with the transition between steps taking 10 seconds and a dwell time of 10 seconds at each step. No changes in image were seen during the dwell period, indicating that the thermally induced strain came into equilibrium on a sub-second timescale. It is of interest to note that negligible bowing of the wafer chip occurred during the power sequence, as the length of the diffraction image in the direction of the diffraction vector stayed almost constant. This was confirmed by a sequence of section topographs (see below) in which the wafer was scanned across a narrow slit. Unlike the heavily warped wafers of references [8], [9] and [10], there was only about 50μm movement of the narrow diffracted image on the detector placed at a distance of 190mm. This indicated that the sample was flat to within about 5 arc seconds across its 1mm length throughout the powering procedure.

There was a substantial change in wafer shape after failure at power dissipation in excess of 2.5W. At power dissipation of 2.4W, the outside of the package reached 210°C and on cooling after failure, the image length increased substantially (Fig 3(d)). The increase in XRDI length arises from a diffraction effect attributable to long range bowing of the wafer and will have been facilitated by the polymer packaging plastically deforming at the high temperature. From the increase in image length in fig. 3(d), we deduce that the wafer bowed to a radius of curvature of about 0.9m. Neither the warpage associated with cooling following heating nor the local strain field from a powered device had any effect on the other transistors in the package. No electrical changes were observed in other transistors after powering an individual transistor to failure.

In the direction normal to the diffraction vector, i.e. horizontal in Fig 3, the length of the region of enhanced diffraction varies monotonically with the power dissipated in the transistor (Fig 4). Beyond a threshold of between 1.3 and 1.5W, the length varies quadratically with the product $V_{CE}I_C$. This variation was reproduced in the other transistors on this and other chips.

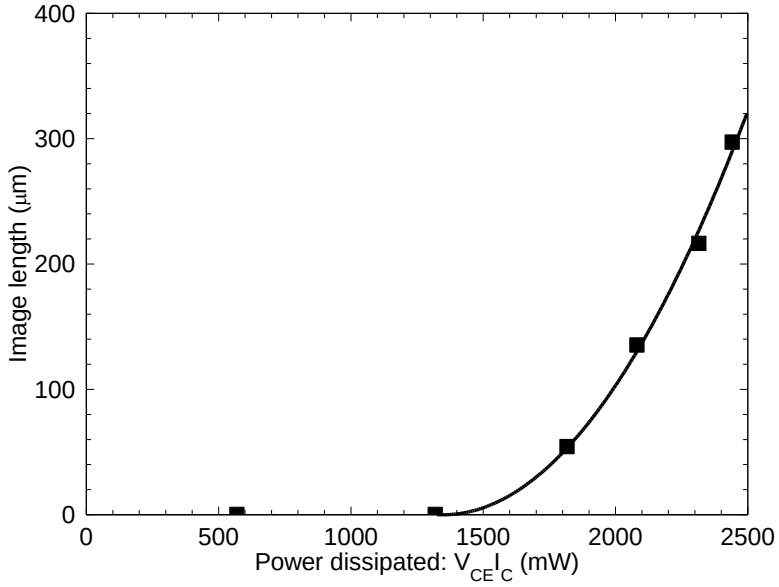
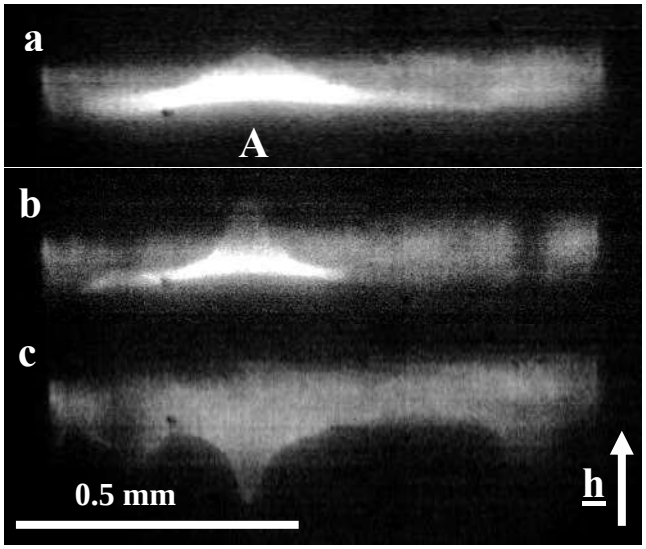


Fig. 4. Length of region of enhanced contrast as a function of power dissipated in the transistor. The solid line is a quadratic fit to the data above a threshold value.

3.2 Section imaging

A standard technique in XRDI, known as section topography, is to use an X-ray beam that is narrow in the direction of the diffraction vector, thereby enabling the variation in strain through the thickness of the wafer to be determined. We used a beam of 7 mm × 15μm and scanned this very narrow beam over the wafer chip in order to determine the change of strain at the transistor when under load. The image changes abruptly on scanning in 50μm steps in the direction of the diffraction vector across the position of the powered transistor. Fig. 5 shows an example of three such sequential steps. Notable is the asterism in the image at the device, marked A, which switches direction, indicating that the lattice tilt switches sign across the device. Such a variation is consistent with the tilt of the crystal lattice planes on opposite sides of the transistor as the transistor heats up during operation. The lattice expands locally, forcing the surrounding planes to tilt as sketched in Fig.5(d). The image of Fig.5(a) corresponds to where the planes are tilted in the direction of the diffraction vector, stretching the diffraction image out in a positive direction. Conversely, in Fig.5(c), the planes are tilted in the opposite direction and the streak appears in the direction opposite to that of the diffraction vector. It should be noted that, if the wafer is undistorted, the diffracted image width will be approximately 100μm, as the 15μm incident beam is spread out by the wafer thickness multiplied by $2\tan\theta_B$ (Fig.5(d)) as the X-ray wave propagates through the crystal. This intrinsic broadening by 85μm is indeed observed, except at the edges of the die, where there is residual damage from the dicing process and the section image is there found to be substantially further broadened.



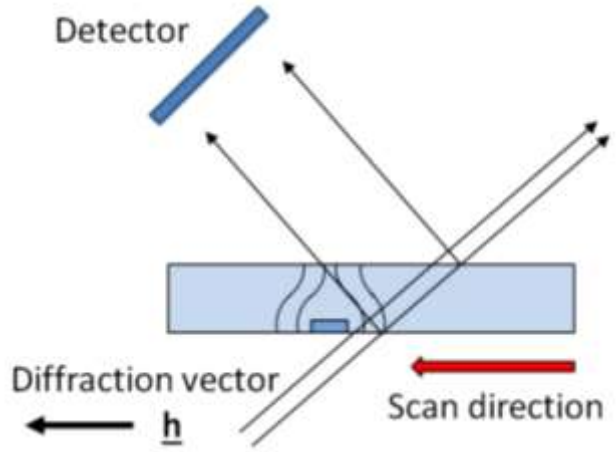


Fig. 5. (a-c) 220 section topographs taken in 50μm steps across the transistor position. The asterism switches sign between the second and third steps. Data taken with the pco4000 X-ray microscope. (d) Schematic diagram of the lattice tilt around the device, deduced from the asterism. [Note that this diagram is oriented at 90° to the images.]

If the slits are located in the lateral position equivalent to that of Fig.5(c), the variation of the lattice plane tilt can be assessed as a function of the power dissipated in the transistor. This is shown in Fig.6. As might be expected, the asterism at the device, again marked A, increases with the load. The length of the streak is proportional to the lattice tilt, which is directly related to the thermal expansion. As for the image in the wide area topographs (Figs.3&4), there is a threshold below which no perceptible change is observed. After the threshold, the asterism length increases linearly (Fig.7). The best fit to the data gives a gradient of $0.30\pm0.02 mmW^{-1}$ with a threshold intercept of 1.3±0.1W.

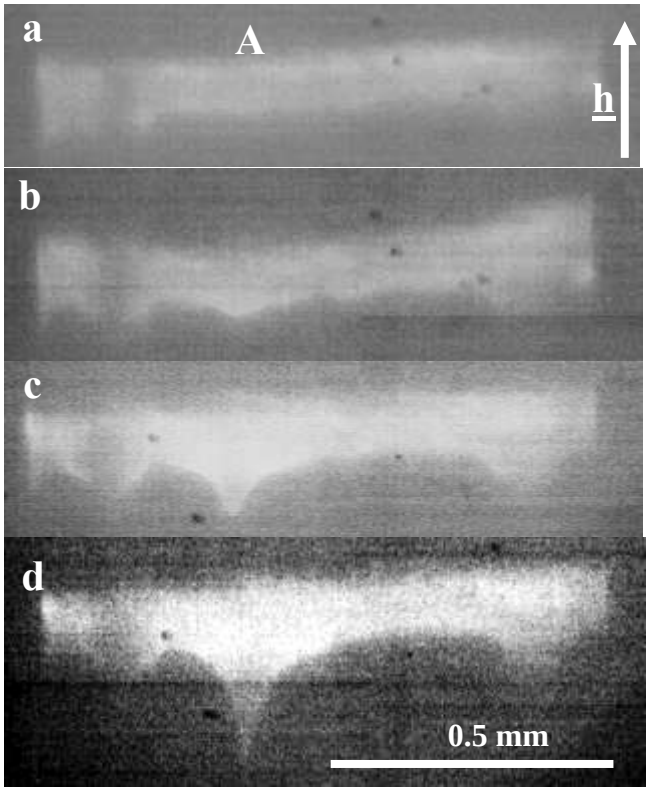


Fig.6. 220 section images with slits situated on one side of the transistor location, corresponding to the image of Fig.5(c), as a function of power through the transistor. (a) 0.57W, (b) 1.32W, (c) 1.8W (d) 2.3W

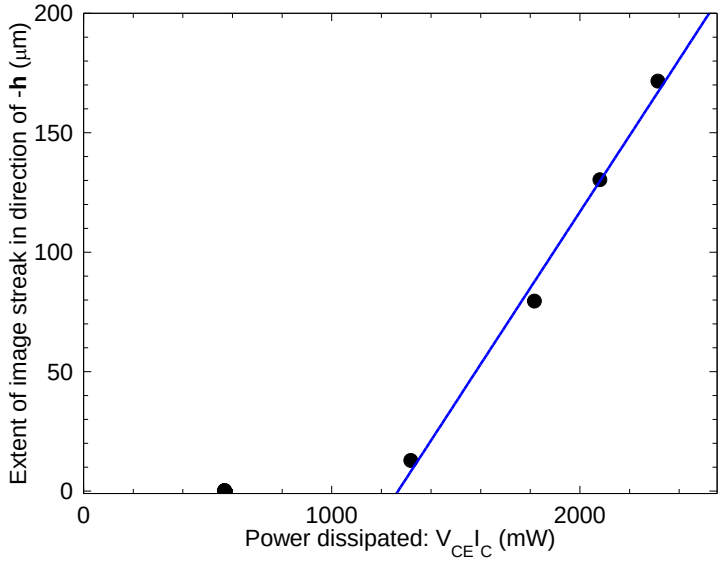


Fig. 7. Asterism streak length in Fig.6 as a function of power dissipated in the transistor.

3.3 Thermal measurements

During the XRDI observations, the outside temperature of the LM3046 package was continuously monitored by the FLIR thermal imaging camera. The temperature change was

found to be remarkably similar for powering of any of the three single transistors in the device and consistent between devices. Fig. 8 shows the variation of the package average outside temperature as a function of power dissipated in the transistors. The linearity and the intercept close to room temperature indicates that there is no significant heating of the package by the X-ray beam.

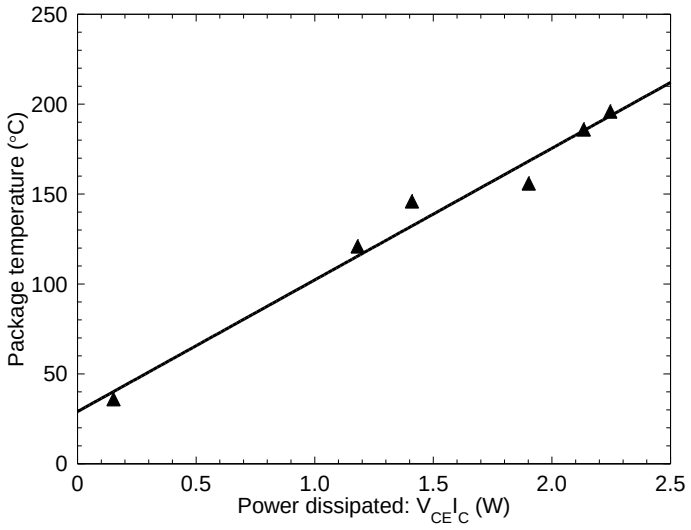


Fig.8. Temperature of the outside of the package as a function of power dissipated in a single transistor. The gradient is 73±6 KW^{-1}

4. Discussion

Because there is very low absorption of X-rays within the silicon wafer chip itself, the image formation is not complicated by dynamical diffraction effects. The enhanced intensity corresponds to the so-called "kinematical image" in XRDI, where the image is formed in the deformed region by X-rays that are not diffracted by the perfect crystal. To a first approximation, the image is formed when the effective misorientation (Equation 1) exceeds the Darwin width, that is the fundamental diffracting range of a perfect crystal. For short wavelength (high energy) X-rays, this width is small and for the 220 reflection in silicon at an X-ray energy of 31keV, it is only 1.2 arc seconds (or 6 μradians). Thus only a small tilt of the Bragg planes due to non-uniform lattice expansion from local heating will give rise to contrast in the image. The power threshold, below which no local contrast is observed, arises because at very low power, no regions satisfy the condition of being tilted by more than 1.2 arc seconds and subsequently, only a small volume of material satisfies this condition, not providing enough enhanced intensity to be detected.

What was unexpected, however, was that as the power load increased, the image extension was unidirectional. If the increase were simply due to thermal expansion associated with the local temperature increase, one would expect there to be a two dimensional expansion of the image. This extension of the image, in only one direction in the large area topograph images as the collector-emitter voltage is increased, is difficult to explain without access to the specific device geometry, on which information is not available. However, it is known that, for a planar device, the emitter-base voltage is not laterally uniform due to the finite resistance of the base region [15]. As the base-emitter current depends exponentially on this voltage, the result is a non-uniform emitter current distribution which, in turn, results in a

non-uniform collector current. This current crowding effect results in non-uniform heating along the device. As the (measured) base-emitter voltage decreases as the series resistor R_L is reduced, the current crowding effect will reduce and the (increased) collector current will flow over a longer length of the device, resulting is an extension of the localised heated region. As remarked above, without details of the exact device geometry, it is difficult to test further the validity of this explanation. The very rapid and catastrophic breakdown when the load resistor is reduced to 100Ω may not triggered so much by damage caused through internal device heating, but rather from avalanche ionization and/or punch-through in the base-collector region. Avalanche breakdown leads to holes generated by impact ionization being pulled into the base region, resulting in increased base and collector currents and hence thermal runaway.

Whatever the exact mechanism, the image length L can be well fitted to a quadratic function in the power dissipated P, in the form

$$L = a(P - P_0)^2 \qquad \text{Equation 2}$$

where the threshold P_0 is allowed as a free fitting parameter and a is a constant. Any fundamental mechanism behind this variation is not apparent and finite element modelling is impossible without information on the device geometry. The threshold values P_0 for image formation in both large area and section topographs are consistent within the experimental precision.

Unlike the quadratic variation of Equation 2, the linear variation (Fig. 7) of the asterism in the section topographs of Fig.6 can be accounted for more straightforwardly. Such asterism has been seen in images of epitaxial lateral overgrowth structures of GaAs, the sense of the asterism being consistent with the sense of the strain in such structures [16]. A similar effect has also been seen in simulated images of silicon device structures [17]. The image width in the large area topographs of Fig.3 does not increase substantially in the direction parallel to the diffraction vector as the power is increased. However, the asterism arises from the distortion of the lattice planes through the depth of the wafer. The thermal expansion will scale with temperature and as the overall package temperature rises linearly with power dissipated (Fig. 8), we may take the local temperature rise also to increase linearly with power. The asterism is not very sensitive to the lattice dilation from the temperature rise, due to the small Bragg angle, but the tilt of the lattice planes will scale proportionally to that dilation. Thus we may expect the extent of the asterism streak in Fig. 6 also to scale linearly with temperature, and hence power, beyond a threshold for local heating, as observed in Fig. 7.

What is needed, if we are to use XRDI to monitor the local temperature of specific components inside a working package, is a measure of the Ψ_{jt} thermal resistance between the die and upper package surface. Noting that the thermal resistance is the inverse of the thermal conductivity, the relevant equation is

$$T_j - T_p = \Psi_{jt} P \qquad \text{Equation 3}$$

where T_j is the local component junction temperature, T_p is the temperature of the top surface of the package and P is the power dissipated.

For the bipolar junction transistor we then have

$$T_j - T_p = \Psi_{jt}(V_{CE} I_C + V_{BE} I_B) \approx \Psi_{jt} V_{CE} I_C \qquad \text{Equation 4}$$

as the base current I_B is small compared with the collector current I_C. (V_{CE} and V_{BE} are the collector-emitter and base-emitter voltage drops respectively.)

The value of Ψ_{jt} has been measured for a variety of package types by workers at the New Japan Radio Co. Ltd. and these include the generic SSOP14 package, which is that used for LM3046 devices [18]. The measurement was achieved by use of a thermocouple to measure the package temperature and a diode and heating resistor fabricated on a custom-made chip within the SSOP14 package. While the resistor was simply used as a heating element, the forward voltage across the diode under constant current conditions was used to measure temperature. (Temperature measurement using diodes in this manner is a standard practice in cryogenic temperature physics experiments.) Their quoted value for Ψ_{jt} is 38 KW^{-1}.

From these measurements, it is now possible to determine the temperature at the component transistors in the LM3046 device from the length of the enhanced contrast in XRDI. Combining the data of Figs. 4 and 8 with the above value for Ψ_{it} we can now plot directly the local temperature as a function of image length (Fig.9). The temperature values are not unreasonable in the context of the short lifetime of the devices under these extreme conditions. Normal permitted operating temperatures for the LM3046 devices range from -40 to 85°C.

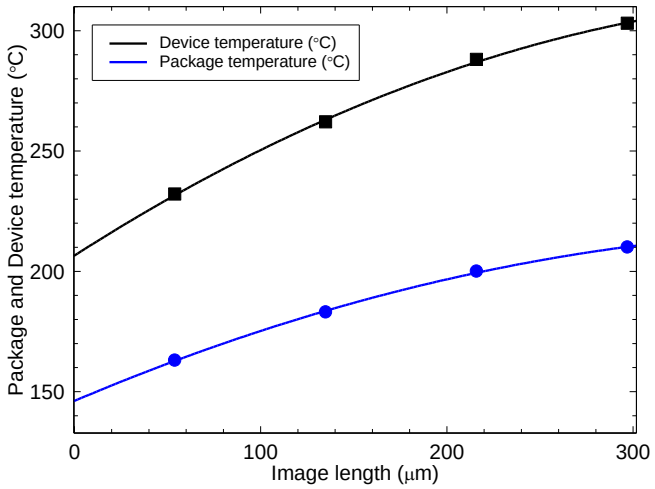


Fig. 9. Plot of package and local transistor temperature as a function of XRDI image length in the LM3046 device. Squares represent the transistor temperature and circles the outside package temperature.

The linear variation of package temperature T_p shown in Fig 8 is consistent with a constant thermal resistance R_{th} between the package and its surroundings at ambient temperature T_a. Again we have an equation similar to equation 4

$$T_p - T_a = R_{th}(V_{CE} I_C + V_{BE} I_B) \approx R_{th} V_{CE} I_C \qquad \text{Equation 5}$$

The value of R_{th} is 73 ± 6 KW^{-1} as measured from the gradient of Fig. 8. This is comparable to other reported values and consistent with the value below, estimated from the various thermal resistance metrics determined by researchers at the New Japan Radio Co. Ltd. for the SSOP14 package [18]. Using their methodology, they have determined θ_{ja} , the thermal resistance between the junction at temperature T_j, and the ambient temperature T_a . As noted above, they also measured Ψ_{jt} , the thermal resistance between the junction at T_j and the temperature of the top surface of the IC package T_p). For the SSOP14 package and under the definitions of θ_{ja} and Ψ_{jt} in [18], we will assume that half the total heat loss is driven to just one side of the package. Then, from [18], an order of magnitude estimate for R_{th} is given by $\frac{1}{2}(\theta_{ja} - \Psi_{jt}) = 93.5$ KW^{-1}. Caveats attach to this estimation, but it is of the same magnitude as given above from our measurements. These estimates are of necessity to order of magnitude because, as noted in [19], the measurement of thermal resistance for a chip package is very dependent on the configuration and size of the test board used by each individual chip/package manufacturer. Hence, data may not be directly comparable between different manufacturers. There is little published literature, and one must rely on manufacturers' data sheets. Comparison with data published by Infineon for their TLE42794 Low Dropout Fixed Voltage Regulator, in the SSOP14 configuration [20] gives an estimate for R_{th} of $\frac{1}{2}(\theta_{ja} - \Psi_{jt})$ = ½ (145 - 10) KW^{-1} = 67.5 KW^{-1} for the simplest 1s0p board layout, i.e. relatively low heat sinking. While heavily caveated, it is consistent with our measurements and not too dissimilar to that of reference [18].

5. Conclusions

The above results provide a proof-of-principle demonstration of the possibility of using X-ray Diffraction Imaging as a means of monitoring the temperature of individual components of a packaged chip during operation. While the above value cannot be immediately transferred to other components and packages, we have shown that calibration is possible and that the localized image does scale with power dissipated in the device. There is a challenge to transfer the technique from a synchrotron radiation source to a laboratory or fabrication facility (fab) environment, but we note that the energy of the Kβ characteristic X-ray line from a commercially available silver (Ag) target is 24.94keV and that this does penetrate SOIC packages such as the LM3046. The intensity of the beam in the Bruker JV Sensus XRDI system might possibly be sufficient for fab-based measurements.

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